Features

- Single 2.7V - 3.6V Supply
- RapidS™ Serial Interface: 66 MHz Maximum Clock Frequency
  - SPI Compatible Modes 0 and 3
- User Configurable Page Size
  - 512 Bytes per Page
  - 528 Bytes per Page
  - Page Size Can Be Factory Pre-configured for 512 Bytes
- Page Program Operation
  - Intelligent Programming Operation
  - 8,192 Pages (512/528 Bytes/Page) Main Memory
- Flexible Erase Options
  - Page Erase (512 Bytes)
  - Block Erase (4 Kbytes)
  - Sector Erase (64 Kbytes)
  - Chip Erase (32 Mbits)
- Two SRAM Data Buffers (512/528 Bytes)
  - Allows Receiving of Data while Reprogramming the Flash Array
- Continuous Read Capability through Entire Array
  - Ideal for Code Shadowing Applications
- Low-power Dissipation
  - 7 mA Active Read Current Typical
  - 25 µA Standby Current Typical
  - 5 µA Deep Power Down Typical
- Hardware and Software Data Protection Features
  - Individual Sector
- Sector Lockdown for Secure Code and Data Storage
  - Individual Sector
- Security: 128-byte Security Register
  - 64-byte User Programmable Space
  - Unique 64-byte Device Identifier
- JEDEC Standard Manufacturer and Device ID Read
- 100,000 Program/Erase Cycles Per Page Minimum
- Data Retention – 20 Years
- Industrial Temperature Range
- Green (Pb/Halide-free/RoHS Compliant) Packaging Options

32-megabit 2.7-volt DataFlash®

AT45DB321D

1. Description

The AT45DB321D is a 2.7-volt, serial-interface sequential access Flash memory ideally suited for a wide variety of digital voice-, image-, program code- and data-storage applications. The AT45DB321D supports RapidS serial interface for applications requiring very high speed operations. RapidS serial interface is SPI compatible for frequencies up to 66 MHz. Its 34,603,008 bits of memory are organized as 8,192 pages of 512 bytes or 528 bytes each. In addition to the main memory, the AT45DB321D also contains two SRAM buffers of 512/528 bytes each. The buffers allow the receiving of data while a page in the main Memory is being reprogrammed, as well as writing a continuous data stream. EEPROM emulation (bit or byte alterability) is easily handled with a self-contained three step read-modify-write operation. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a RapidS serial interface to

sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage and low-power are essential.

To allow for simple in-system reprogrammability, the AT45DB321D does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB321D is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming and erase cycles are self-timed.

2. Pin Configurations and Pinouts

Figure 2-1. MLF[1] (VDFN) Top View

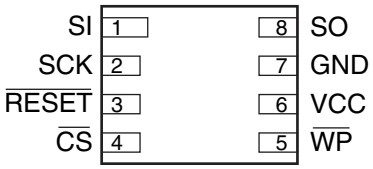
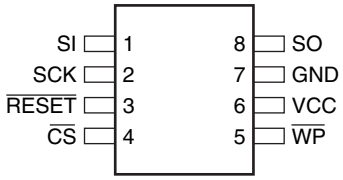
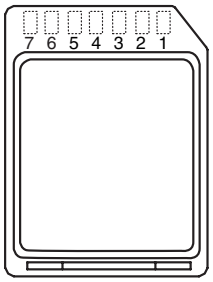


Figure 2-2. SOIC Top View



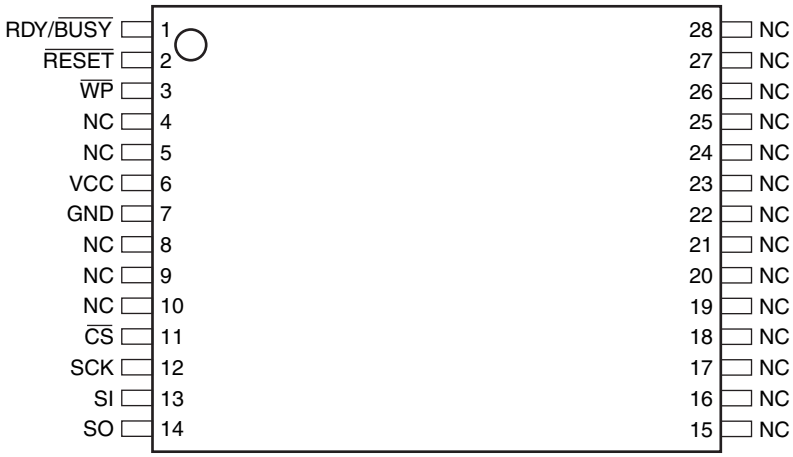
Note: 1. The metal pad on the bottom of the MLF package is floating. This pad can be a “No Connect” or connected to GND.

Figure 2-3. DataFlash Card[1]
Top View through Package



Note: 1. See AT45DCB004D Datasheet.

Figure 2-4. TSOP Top View: Type 1



Note: TSOP package is not recommended for new designs. Future die shrinks will support 8-pin packages only.

18. Electrical Specifications

Table 18-1. Absolute Maximum Ratings*

Temperature under Bias	-55° C to +125° C
Storage Temperature	-65° C to +150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 18-2. DC and AC Operating Range

		AT45DB321D
Operating Temperature (Case)	Ind.	-40° C to 85° C
V_{CC} Power Supply		2.7V to 3.6V

Table 18-3. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DP}	Deep Power-down Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		5	10	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		25	50	µA
I_{CC1} (1)	Active Current, Read Operation	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		7	10	mA
		f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		8	12	mA
		f = 50 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		10	14	mA
		f = 66 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		11	15	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		12	17	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

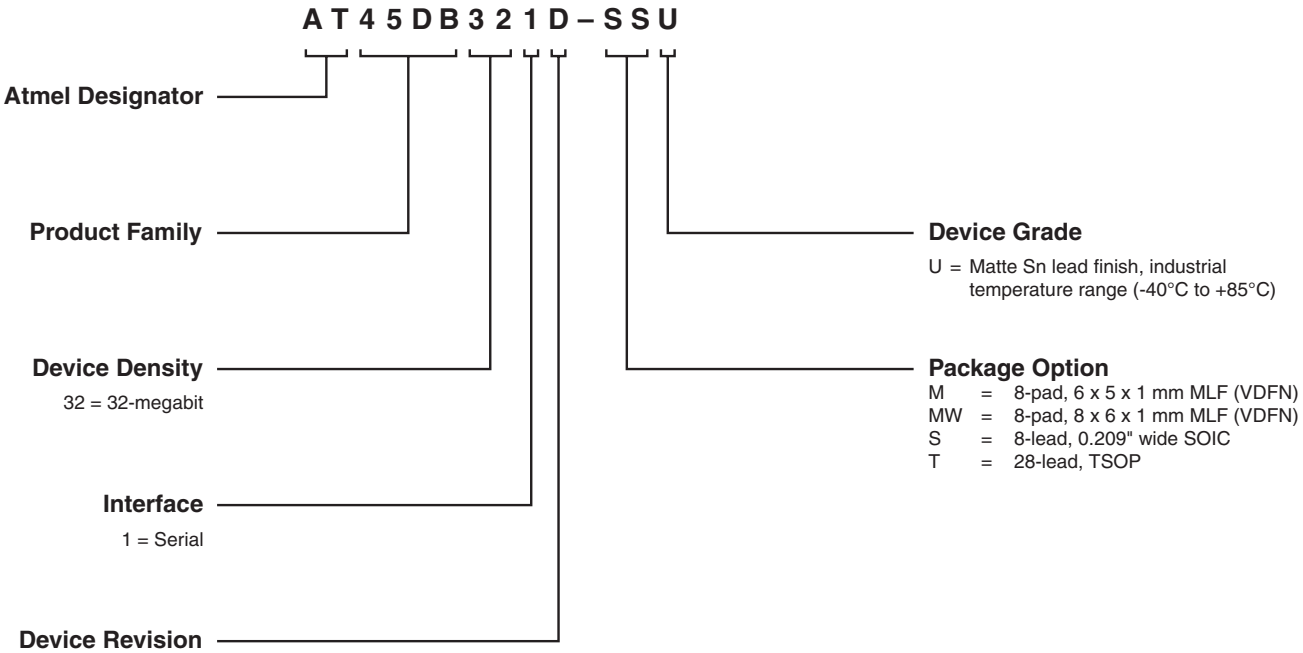
Notes: 1. I_{CC1} during a buffer read is 20 mA maximum @ 20 MHz.
2. All inputs are 5 volts tolerant.

Table 18-4. AC Characteristics – RapidS/Serial Interface

Symbol	Parameter	AT45DB321D			
		Min	Typ	Max	Units
f_{SCK}	SCK Frequency			66	MHz
f_{CAR1}	SCK Frequency for Continuous Array Read			66	MHz
f_{CAR2}	SCK Frequency for Continuous Array Read (Low Frequency)			33	MHz
t_{WH}	SCK High Time	6.8			ns
t_{WL}	SCK Low Time	6.8			ns
t_{SCKR}[1]	SCK Rise Time, Peak-to-Peak (Slew Rate)	0.1			V/ns
t_{SCKF}[1]	SCK Fall Time, Peak-to-Peak (Slew Rate)	0.1			V/ns
t_{CS}	Minimum $\overline{CS}$ High Time	50			ns
t_{CSS}	$\overline{CS}$ Setup Time	5			ns
t_{CSH}	$\overline{CS}$ Hold Time	5			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			100	ns
t_{SU}	Data In Setup Time	2			ns
t_{H}	Data In Hold Time	3			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			6	ns
t_{V}	Output Valid			6	ns
t_{WPE}	$\overline{WP}$ Low to Protection Enabled			1	µs
t_{WPD}	$\overline{WP}$ High to Protection Disabled			1	µs
t_{EDPD}	$\overline{CS}$ High to Deep Power-down Mode			3	µs
t_{RDPD}	$\overline{CS}$ High to Standby Mode			35	µs
t_{XFR}	Page to Buffer Transfer Time			200	µs
t_{comp}	Page to Buffer Compare Time			200	µs
t_{EP}	Page Erase and Programming Time (512/528 bytes)		17	40	ms
t_{P}	Page Programming Time (512/528 bytes)		3	6	ms
t_{PE}	Page Erase Time (512/528 bytes)		15	35	ms
t_{BE}	Block Erase Time (4,096/4,224 bytes)		45	100	ms
t_{CE}	Chip Erase Time		TBD	TBD	s
t_{SE}	Sector Erase Time (262,144/270,336 bytes)		1.6	5	s
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

26. Ordering Information

26.1 Ordering Code Detail



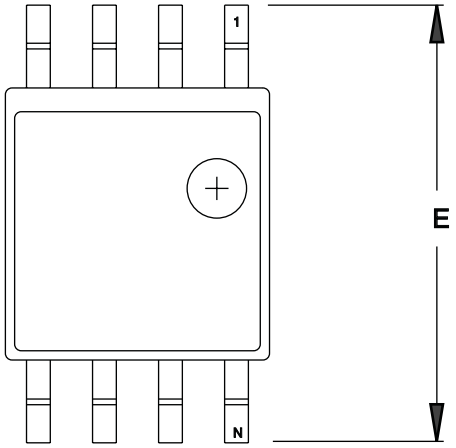
26.2 Green Package Options (Pb/Halide-free/RoHS Compliant)

Ordering Code[1][2]	Package	Lead Finish	Operating Voltage	f_{SCK} (MHz)	Operation Range
AT45DB321D-MU AT45DB321D-MU-SL954[3] AT45DB321D-MU-SL955[4]	8M1-A	Matte Sn	2.7V to 3.6V	66	Industrial (-40° C to 85° C) 2.7V to 3.6V
AT45DB321D-MWU AT45DB321D-MWU-SL954[3] AT45DB321D-MWU-SL955[4]	8MW				
AT45DB321D-SU AT45DB321D-SU-SL954[3] AT45DB321D-SU-SL955[4]	8S2				
AT45DB321D-TU	28T				

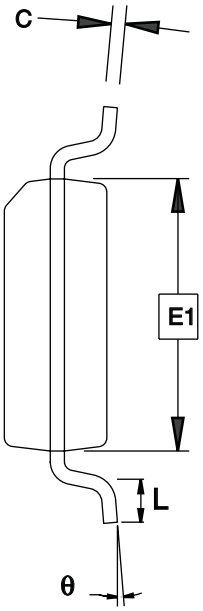
Notes:
1. The shipping carrier option is not marked on the devices.
2. Standard parts are shipped with the page size set to 528 bytes. The user is able to configure these parts to a 512-byte page size if desired.
3. Parts ordered with suffix SL954 are shipped in bulk with the page size set to 512 bytes. Parts will have a 954 or SL954 marked on them.
4. Parts ordered with suffix SL955 are shipped in tape and reel with the page size set to 512 bytes. Parts will have a 954 or SL954 marked on them.

Package Type	
8M1-A	8-pad, 6 x 5 x 1.0 mm, Very Thin Micro Lead-frame Package MLF™ (VDFN)
8MW	8-pad, 8 x 6 x 1.0 mm, Very Thin Micro Lead-frame Package MLF (VDFN)
8S2	8-lead, 0.209" wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
28T	28-lead, 8 mm x 13.4 mm, Plastic Thin Small Outline Package, Type I (TSOP)

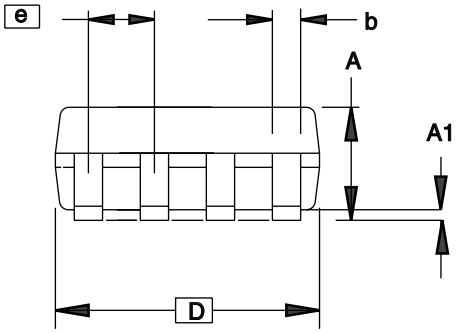
27.3 8S2 – EIAJ SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	5
C	0.15		0.35	5
D	5.13		5.35	
E1	5.18		5.40	2, 3
E	7.70		8.26	
L	0.51		0.85	
θ	0°		8°	
e	1.27 BSC			4

Notes:
1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs are not included.
3. It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.
4. Determines the true geometric position.
5. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8S2**, 8-lead, 0.209" Body, Plastic Small Outline Package (EIAJ)	8S2	D